LISTING OF THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) A timing adjustment circuit, comprising:

an input circuit ~~for outputting~~ effective to receive an external clock signal ~~supplied from the outside as~~ and output an input clock signal;

a delay adjustment circuit ~~for delaying~~ effective to delay the input clock signal from the input circuit to output a delayed input clock signal; and

a clock driver ~~for outputting~~ effective to output an internal clock signal to a data output circuit in response to the delayed input clock signal from the delay adjustment circuit, ~~so as to determine delay of the delay adjustment circuit~~ so that a phase of an output signal outputted from ~~a~~ the data output circuit ~~to be driven in synchronization with the internal clock signal~~ has a predetermined relation with respect to that of the external clock signal~~, when the internal clock signal is used to drive the circuit to be driven,~~

~~the timing adjustment circuit further comprising~~ a phase advance/delay signal generation unit, the phase advance/delay signal generating unit effective to selectively compare ~~for using~~ the internal clock signal and either one of the external clock signal and the output signal of the data output circuit ~~to be driven~~ to produce a phase advance/delay signal indicating whether the phase of the output signal ~~from~~ of the data output circuit ~~to be driven~~ advances or delays with respect to the phase of the external clock signal;

a phase comparison circuit for comparing the phase of the output signal of the replica circuit with that of the external clock signal and outputting a comparison result to the delay adjustment circuit to adjust the delay of the delay adjustment circuit; and

an external output unit for outputting an output of the phase comparison circuit to the outside,

wherein the comparison result of the phase comparison circuit is supplied as the phase advance/delay signal to the external output unit.

2. (Canceled)

3. (Currently Amended) The timing adjustment circuit according to claim 2, wherein:

the replica circuit is effective to delay the internal clock signal based on a ~~constituted to be capable of adjusting a delay time by~~ change of a content held in a register or by disconnection of a fuse.

4. (Currently Amended) A semiconductor device, comprising:

~~the timing adjustment circuit according to claim 1; and~~

an input circuit effective to receive an external clock signal and output an input clock signal;

a delay adjustment circuit effective to delay the input clock signal from the input circuit to output a delayed input clock signal; and

a clock driver effective to output an internal clock signal to a data output circuit in response to the delayed input clock signal from the delay adjustment circuit, so that a phase of an output signal outputted from ~~a~~ the data output circuit has a predetermined relation with respect to that of the external clock signal; and

a phase advance/delay signal generation unit, the phase advance/delay signal generating unit effective to selectively compare the internal clock signal and either one of the external clock signal and the output signal of the data output circuit to produce a phase advance/delay signal indicating whether the phase of the output signal of the data output circuit advances or delays with respect to the phase of the external clock signal

~~a data output circuit for functioning as a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit to output data at a timing defined by the internal clock signal~~.

5. (Currently Amended) A semiconductor device, comprising:

an input circuit effective to receive an external clock signal and output an input clock signal;

a delay adjustment circuit effective to delay the input clock signal from the input circuit to output a delayed input clock signal; and

a clock driver effective to output an internal clock signal to a data output circuit in response to the delayed input clock signal from the delay adjustment circuit, so that a phase of an output signal outputted from a the data output circuit has a predetermined relation with respect to that of the external clock signal; and

a phase advance/delay signal generation unit, the phase advance/delay signal generating unit effective to selectively compare the internal clock signal and either one of the external clock signal and the output signal of the data output circuit to produce a phase advance/delay signal indicating whether the phase of the output signal of the data output circuit advances or delays with respect to the phase of the external clock signal;

a replica circuit effective to receive and delay the internal clock signal, the replica circuit being effective to delay the internal clock signal based on a change of a content held in a register or by disconnection of a fuse;

wherein the phase advance/delay signal generating unit compares the internal clock signal delayed by the replica circuit; and

the phase advance/delay signal generating unit includes a selection circuit effective to selectively output either one of the external clock signal and the output signal from the data output circuit to the phase comparison circuit;

~~the timing adjustment circuit according to claim 3 capable of adjusting both a delay time by change of a content held by a register and a delay time by disconnection of a fuse; and~~

~~a data output circuit for outputting data at a timing defined by the internal clock signal, which is a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit,~~

~~wherein~~ whereby when a tester is connected to ~~the external output unit is used to~~ monitor the phase advance/delay signal ~~while~~ and the content held by the register is changed to obtain an appropriate delay time, ~~and subsequently~~ the fuse ~~is~~ may be disconnected so that a ~~the~~ delay time

of the semiconductor device ~~timing adjustment circuit~~ can be fixed ~~to the appropriate delay time~~.

6. (Currently Amended) The timing adjustment circuit according to claim 1, wherein:

~~the delay adjustment circuit is constituted to be capable of changing the delay time,~~

the data output circuit ~~to be driven is a data input circuit for latching~~ includes a latch effective to latch input data ~~supplied from the outside~~ in synchronization with the internal clock signal, and

the phase advance/delay signal generation unit includes ~~the same constitution~~ a similar impedance as that of the data output circuit ~~to be driven~~ and ~~comprises a unit for receiving supply of~~ is effective to receive the external clock signal ~~instead of the input data~~ and to latch the external clock signal in synchronization with the internal clock signal and for outputting the phase advance/delay signal to the outside.

7. (Currently Amended) The timing adjustment circuit according to claim 6, wherein:

the delay adjustment circuit is ~~constituted to be capable of adjusting~~ effective to delay the input clock signal ~~the delay time~~ by change of a content held by a register or by disconnection of a fuse.

8. (Currently Amended) A semiconductor device, comprising:

~~the timing adjustment circuit according to claim 6 ; and~~

an input circuit effective to receive an external clock signal and output an input clock signal;

a delay adjustment circuit effective to delay the input clock signal from the input circuit to output a delayed input clock signal; and

a clock driver effective to output an internal clock signal to a data output circuit in response to the delayed input clock signal from the delay adjustment circuit, so that a phase of an output signal outputted from a the data output circuit has a predetermined relation with respect to

that of the external clock signal; and

a phase advance/delay signal generation unit, the phase advance/delay signal generating unit effective to selectively compare the internal clock signal and either one of the external clock signal and the output signal of the data output circuit to produce a phase advance/delay signal indicating whether the phase of the output signal of the data output circuit advances or delays with respect to the phase of the external clock signal;

the data output circuit includes a latch effective to latch input data in synchronization with the internal clock signal, and

the phase advance/delay signal generation unit includes a similar impedance as that of the data output circuit and is effective to receive the external clock signal and to latch the external clock signal in synchronization with the internal clock signal;

~~a data input circuit for latching input data supplied from the outside at a timing defined by the internal clock signal, which is a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit~~.

9. (Currently Amended) A semiconductor device as recited in claim 8, ~~comprising~~ wherein:

the delay adjustment circuit is effective to delay the input clock signal by change of a content held by a register or by disconnection of a fuse;

~~the timing adjustment circuit according to claim 7 capable of adjusting both a delay time by change of a content held by a register and a delay time by disconnection of a fuse; and~~

~~a data input circuit for latching input data supplied from the outside at a timing defined by the internal clock signal, which is a circuit to be driven by an internal clock signal supplied from the timing adjustment circuit,~~

~~wherein~~ whereby when a tester is connected to ~~the phase advance/delay signal generation unit is used to~~ monitor the phase advance/delay signal and ~~while~~ the content held by the register is changed to obtain an appropriate delay time, ~~and subsequently~~ the fuse ~~is~~ may be disconnected so that ~~the~~ a delay time of the ~~timing adjustment circuit~~ semiconductor device can be fixed ~~to the appropriate delay time~~.